



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,081	01/20/2004	Chou H. Li	2480.202	7150

7590 12/16/2005

Matthew A. Pequignot, Esquire
Hall, Priddy, Myers & Vande Sande
Ste. 200
10220 River Road
Potomac, MD 20854


EXAMINER

WILSON, ALLAN R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/759,081	Applicant(s) LI, CHOU H.	
	Examiner Allan R. Wilson	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,6,8,10,15,16,18-20,23-26,28,30-34,36,38,45,46,48-50 and 56-61 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Continuation of Disposition of Claims: Claims pending in the application are 1,3,5,6,8,10,15,16,18-20,23-26,28,30-34,36,38,45,46,48-50 and 56-61.

DETAILED ACTION

Election/Restrictions

Applicant's election of Species II on September 29, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3, 5, 6, 8, 10, 15, 16, 18-20, 23-26, 28, 30-34, 36, 38, 45, 46, 48-50 and 56-61 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 44-53 of copending Application No. 08/483,938. Although the conflicting claims are not identical, they are not patentably distinct from each other because, for

Art Unit: 2815

example, the present application's claim 1 is broader than claim 44 of the '938 patent. The present application's claim 1 contains the same limitations as claim 44 of the '938 patent except "the barrier region having a selected surface which is microscopically precise, better than one micron in accuracy in shape size, and position or the rectifying barrier; on a vertical cross-section, said barrier region having a curved portion in a major central portion thereof" which can be added to the open claim 1.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 20 recites "a terminal portion" in line 17. There is insufficient antecedent basis for this limitation in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 5, 20, 23-26, 28, 30-34, 36, 38 and 57-74 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The structure which goes to make up

Art Unit: 2815

the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative device.

Claims 3 and 20, the phrase “accuracy of a few hundred atomic layers” is indefinite. The size of the dimension is unclear.

Claim 5 recites the limitation “said number being selected :from the group consisting of one, two, and three” in the last two lines. There is insufficient antecedent basis for this limitation in the claim.

Claim 57, last paragraph, “a major portion of a top surface area of device chip being occupied by device circuit elements themselves thereby achieving hitherto impossible, device miniaturization” is unclear.

Claims 23-26, 28, 30-34, 36, 38 and 58-74 are rejected as being depended on rejected claims 20 and 57.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5, 6, 8, 10, 18-20, 22-26, 28, 30-32, 34, 36, 38, 45, 46, 48-50, 56-58, 60, 63, 65, 67, 72 and 73 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 4,916,716 to Fenner et al. (“Fenner”).

With regards to claim 1, Fenner illustrates in figures 1 and 2 (entire document) a solid substrate 2, 3 of one conductivity type n; a solid material pocket 4 of a different conductivity

Art Unit: 2815

type p having a side surface and positioned on a selected top surface of said substrate; signal-translating, electronic rectifying barrier 3/4 between said solid material pocket and the selected top surface of said substrate; and a solid state material region 7 adjoining said solid substrate, said electronic rectifying barrier, and the side surface of said solid material pocket.

With regards to claim 1, it would have been obvious for the limitation “said solid state material region having a depth accuracy of better than 0.13 microns; and said solid state material region being continuously and perfectly bonded metallurgically to all said solid substrate, said solid material pocket, and said rectifying barrier, without thermally and electrically insulating voids and microcracks visible at 1,000 times magnification in interfacial bonding regions between the device components” since a device has the properties which meet the claimed limitation once the claimed materials and structure are present. Since the claimed material and structure limitation are met by Fenner, the limitation relating to the properties of the layers are also met as a natural result. Fenner discloses in col. 2, lines 65-68, solid state material region 7 (channel or guard ring) is produced by ion implantation of oxygen. This is the same material and process used by Applicant.

With regards to claims 3 and 30, it would have been inherent for the limitation “a lateral edge or at least one of said solid substrate, said solid material pocket, and said electronic rectifying barrier has; a lateral dimensional accuracy of a few hundred atomic layers” since a device has the properties which meet the claimed limitation once the claimed materials and structure are present. Since the claimed material and structure limitation are met by Fenner, the limitation relating to the properties of the layers are also met as a natural result. Fenner discloses in col. 2, lines 65-68, solid state material region 7 (channel or guard ring) is produced by ion

Art Unit: 2815

implantation of oxygen. Applicants in paragraph 133 state that Keller et al. (U.S. Patent No. 3,341,754) discloses implanted region may be controlled with great accuracy down to some few hundred atomic layers.

With regards to claims 5 and 6, Fenner illustrates in FIG. 1 a selected significant portion of a major surface of said solid state material region 7 gradually changes a vertical thickness thereof with closeness in a lateral direction to a lateral edge of said electronic rectifying barrier 3/4.

With regards to claims 8 and 10, Fenner illustrates in FIG. 1 at least a major surface said solid material pocket 7 is curved over a major portion thereof.

With regard to claim 18, a laterally-extending dimension of less than one micron is generally recognized as being within the level of ordinary skill in the art.

With regards to claims 19, 28, 38 and 58, Fenner discloses said solid state material region 7 consists essentially of oxide, metal and electrically insulating solid (Fenner col. 2, lines 65-68); said electronic rectifying barrier 3/4 is selected from the group consisting of a PN junction and a Schottky barrier; and said solid material pocket is GaAs.

With regards to claim 20, Fenner illustrates in FIG. 1 a first semiconductor material body 4 having a first polarity "p"; a second semiconductor material body 3 located generally vertically underneath said first semiconductor material body and having a second polarity "n" that is opposite the first polarity; a signal-translating, electronic rectifying barrier 3/4 formed between said first and second semiconductor material bodies; and a third solid state material body 7 having an electrical conductivity at least one order of magnitude different from those of said first and second semiconductor material bodies (inherent); said third solid state material body

Art Unit: 2815

contacting respective portions of each of said first and second semiconductor material bodies and said electronic rectifying barrier, and having two differentially surface-expanded sides that are not parallel to each other to form a terminal portion of no more than a micron in thickness in a selected direction; and said thickness being accurate to within a few hundred atomic layers (see claim 3 above).

With regards to claim 22, Fenner discloses in col. 2, lines 57-59, said second semiconductor material body 3 is of an intrinsic semiconductor material (weakly n-conductive).

With regards to claim 23, Fenner discloses in col. 2, lines 65-68, said third solid state material body 7 has an as-formed metallurgically graded-seal continuity of a graded-seal type with respect to at least one of said first 4 and second 3 semiconductor material bodies (see claim 3 above).

With regards to claims 24 and 56, Fenner discloses in col. 2, lines 57-60, the terminal portion of said third solid state material body 7 is vertically within less than a distance from a selected point inside said electronic rectifying barrier; said distance being one micron since the thickness of layer 3 can be as thin as 0.2 μm .

With regards to claim 25, since Fenner illustrates in FIG. 1 the third solid state material body 7 has the same geometry, position, and orientation relative to said first 4 and second 3 semiconductor material bodies, it will allow adequate stress and strain modification on said electronic rectifying barrier thereby improving device performance.

With regards to claim 26, Fenner illustrates in FIG. 1 said third solid state material body 7 is favorably stressed, and has a blunt and rounded bottom of zero width and a the rounded

Art Unit: 2815

bottom of said third solid state material body is located within one micron from a designated point inside said electronic rectifying barrier (see claim 24).

With regards to claim 31, Fenner illustrates in FIG. 1 said third solid state material body 7 has a rounded portion forming an inverted arch.

With regards to claim 32, Fenner illustrates in FIG. 1 the terminal portion of said third solid state material body is zero in the lateral direction.

With regards to claim 34, Fenner illustrates in FIG. 2 said third solid state material body 7 has a cylindrical surface.

With regards to claim 36, the limitation "said electronic rectifying barrier is stressed to improve a performance of said semiconductor device" is an inherent function of the structure and since the prior art has the same structure and materials as the claimed invention it will have the same inherent function.

With regards to claim 45, Fenner illustrates in FIG. 1 said electronic rectifying barrier 3, 4 adjoins both said solid substrate 3 and said solid state material region 7 at a place where a periphery of said electronic rectifying barrier is differentially surface-expanded.

With regards to claim 46, Fenner illustrates in FIG. 1 said solid state material region is size with an accuracy of less than 0.13 microns (see claim 3), and having a bottom of a shape selected from the group consisting of rounded, cylindrical or hemispherical.

With regards to claims 48, 49 and 50, Fenner illustrates in FIG. 1 said electronic rectifying barrier 3, 4 has a lateral edge, and said solid state material region 7 has a portion thereof which gradually and continuously changes its vertical thickness with closeness to said lateral edge of said electronic rectifying barrier.

With regards to claim 57, Fenner illustrates in FIG. 1 a first solid state material 4 of a first conductivity type "p", a second solid state material 3 of a second conductivity type positioned under the first solid state material, the first and second solid state materials having respective adjoining portions; a signal-translating, rectifying barrier region 3/4 lying between the respective adjoining portions; and a device material region 7 starting at least in the first solid state material and extending toward the rectifying barrier region to form a bottom which is within a micron (see claim 24) of a selected point inside the rectifying barrier region; a major portion of a top surface area of device chip being occupied by device circuit elements themselves thereby achieving hitherto impossible, device miniaturization.

With regards to claim 60, Fenner illustrates in FIG. 1 the device material region 7 is an elongated device material region; is accurate to less than a micron (see claim 3) in a dimension selected from the group consisting of shape, size, depth, and chemical composition profiling; and consists essentially of a device material selected from the group consisting essentially of oxide, metal, other electrically insulating material (Fenner col. 2, lines 65-68).

Regarding claim 63, Fenner illustrates in FIG. 1 only a minor portion of a top surface area of device chip is not occupied by device circuit elements themselves; said device circuit elements having no centrally large and flat bottoms as in oxidized isolation bottoms of Peltzer and Murphy devices, thereby achieving radically improved device miniaturization.

With regards to claim 65, Fenner illustrates in FIG. 1 the device material region 7 is an elongated, cylindrical device material groove having both an aspect ratio of over 3 to 5 (within one of ordinary skill of the art) and a cylindrical radius of less than one micron, and is oriented generally normally of a top surface of the second solid state material 3.

Art Unit: 2815

With regards to claim 67, the cylindrical size is generally recognized as being within the level of ordinary skill in the art.

With regards to claim 72, Applicant is reminded that intended functional use is given no patentable weight in claims drawn to structure. See *In re Pearson* 181 USPQ 641 and *Ex parte Minks* 169 USPQ 120.

Regarding claim 73, Fenner illustrates in FIG. 1 the device material region 7 is a vertical and electrically insulating, elongated device material groove; and a lower end of the vertical, elongated groove has a centrally rounded bottom of substantially zero width in a direction parallel to a top major surface of the second solid state material.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: MacRae (illustrates implantation of oxygen or nitrogen), Nishizawa et al. (illustrates an insulation layer deposited with MO-CVD) and Japanese Patent Application No. 58-111345 (illustrates a PN junction with an implantation of oxygen).

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
December 12, 2005